

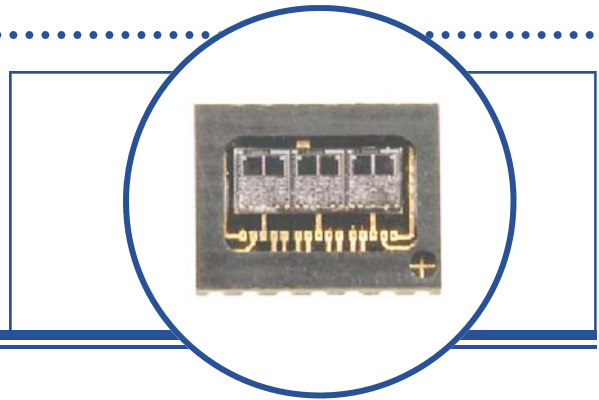
# Optical Comparator Array

## OPR5011



### Features:

- Precise active area location
- Surface mountable
- TTL compatible output
- Wide supply voltage range
- Wide operating temperature range



### Description:

Each **OPR5011** device is a hybrid sensor array that consists of three channels of the OPTEK OPC8332 differential optical comparator ("TRI-DOC") IC. The single chip construction ensures very tight dimensional tolerances between active areas.

Specifically designed for high-speed/high-resolution encoder applications, the open collector output switches based on the comparison of the input photodiode's light current levels. Logarithmic amplification of the input signals facilitates operation over a wide range of light levels.

The surface-mountable opaque polyimide package shields the photodiodes from stray light and can withstand multiple exposures to the most demanding soldering conditions, while the gold-plated wraparound contacts provide exceptional storage and wetting characteristics.

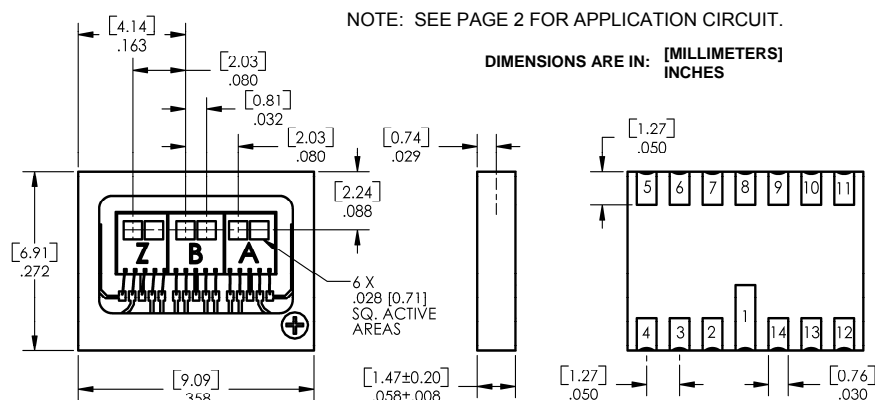
See Application Bulletin 237 for handling instructions.

### Applications:

- High-speed applications
- High-resolution applications
- Applications requiring a wide range of light levels

Ordering Information						
Part Number	Sensor	# of Elements	Icc (mA) Typ / Max	Optical Hysteresis (%) Typical	Optical Offset (%) Min / Max	Packaging
OPR5011	Differential Optical Comparator	3	9 / 20	40.00	-40/+40	Chip Tray

**Warning:** Front Window is pressure sensitive. Do not apply pressure or high vacuum to window.



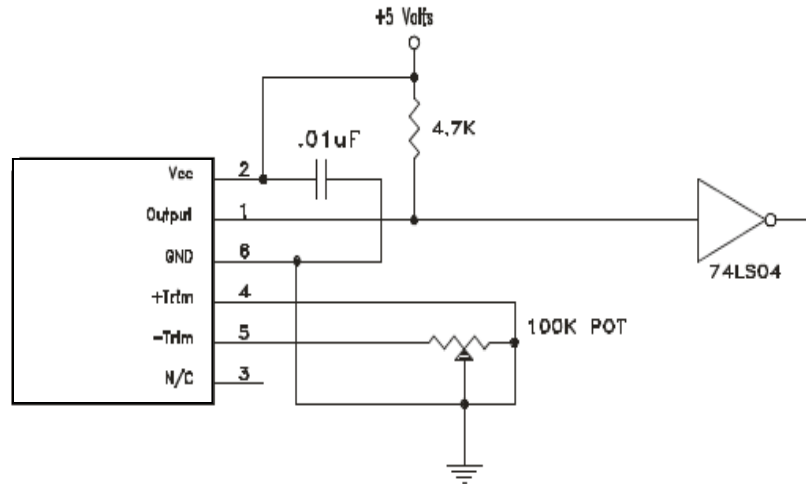
Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description
1	B - Output	5	N.C.	9	Z + Trim	13	B + Trim
2	B - Vcc	6	A - Output	10	Z - Trim	14	B - Trim
3	A + Trim	7	A - Vcc	11	Z - Output		
4	A - Trim	8	Common	12	Z - Vcc		



RoHS

OPTEK reserves the right to make changes at any time in order to improve design and to supply the best product possible.

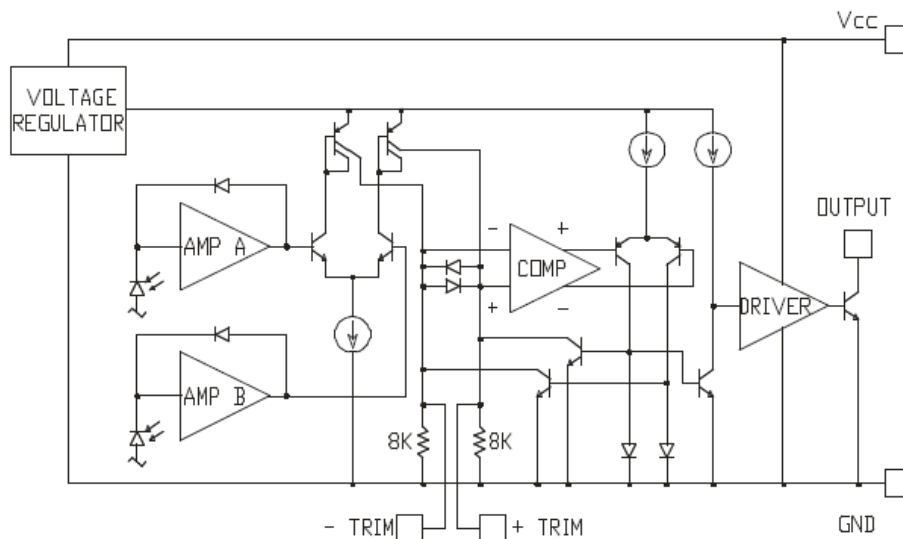
**Application Circuit - OPR5011**



**Notes:**

- (1) The 74LS04 is recommended as a means of isolating the "DOC" comparator circuitry from transients induced by inductive and capacitive loads.
- (2) It is recommended that a decoupling capacitor be placed as close as possible to the device.

**Block Diagram - OPC8332**



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**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Storage and Operating Temperature	-40° C to +100° C
Supply Voltage	24 V
Output Voltage	24 V
Output Current	14 mA
Power Dissipation	500 mW
Solder reflow time within 5°C of peak temperature is 20 to 40 seconds <sup>(1)</sup>	250° C

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
$I_{CC}$	Supply Current	-	9	20	mA	$V_{CC} = 24\text{ V}$
$V_{OL}$	Low Level Output Voltage <sup>(2)</sup>	-	0.3	0.4	V	$I_{OL} = 14\text{ mA}$ , $V_{CC} = 4.5\text{ V}$
$I_{OH}$	High Level Output Current <sup>(3)</sup>	-	0.1	1	$\mu\text{A}$	$V_{CC} = V_O = 20\text{ V}$
OPT-HYS	Optical Hysteresis <sup>(4)(7)</sup>	-	40	-	%	$V_{CC} = 5\text{ V}$ , $I_{OL} = 1\text{ mA}$
OPT-OFF	Optical Offset <sup>(4)(7)</sup>	-40	10	+40	%	$V_{CC} = 5\text{ V}$ , $I_{OL} = 1\text{ mA}$
$f_{max}$	Frequency Response <sup>(5)</sup>	-	1	-	MHz	$V_{CC} = 5\text{ V}$
$t_{rh}$	Output Rise Time <sup>(6)</sup>	-	1	-	$\mu\text{s}$	
$t_{hl}$	Output Fall Time <sup>(6)</sup>	-	300	-	ns	

Notes:

- (1) Solder time less than 5 seconds at temperature extreme.
- (2) Pin (+) = 100.0 nW and Pin (-) = 1.0  $\mu\text{W}$ .
- (3) Pin (+) = 1.0  $\mu\text{W}$  and Pin (-) = 100.0 nW.
- (4) Pin (-) is held at 1.0  $\mu\text{W}$  while Pin (+) is ramped from 0.5  $\mu\text{W}$  to 1.5  $\mu\text{W}$  and back to 0.5  $\mu\text{W}$ .
- (5) Pin (+) is modulated from 1.0  $\mu\text{W}$  to 2.0  $\mu\text{W}$ . Pin (-) is modulated from 1.0  $\mu\text{W}$  to 2.0  $\mu\text{W}$  with phase shifted 180° with respect to Pin (+). Use 100 k $\Omega$  trimpot to set the output signal to 50% duty cycle for maximum operating frequency.
- (6) Measured between 10% and 90% points.
- (7) Optical Hysteresis and Optical Offset are found by placing 1.0  $\mu\text{W}$  of light on the inverting photodiode and ramping the light intensity of the non-inverting input from 0.5  $\mu\text{W}$  up to 1.5  $\mu\text{W}$  and back down. This will produce two trigger points – an upper trigger point and lower trigger point. These points are used to calculate the optical hysteresis and offset.

These are defined as:

$$\% \text{ Optical Hysteresis} = 100 \times \frac{(P_{\text{rise}} - P_{\text{fall}})}{P_{\text{in (-)}}}$$

$$\% \text{ Optical Offset} = \frac{100 \times (P_{\text{average}} - P_{\text{(-)}})}{P_{\text{in (-)}}$$

Where:

$P_{\text{in (-)}}$  = Light level incident upon the “-” photodiode on the IC chip ( $P_{\text{in (-)}}$ ) = 1.0  $\mu\text{W}$ ).

$P_{\text{rise}}$  = Value of light power level incident upon the “+” photodiode that is required to switch the digital output when the light level is an increasing level (rising edge).

$P_{\text{fall}}$  = Value of light power level incident upon the “+” photodiode that is required to switch the digital output when the light level is decreasing level (falling edge).

$$P_{\text{average}} = \frac{(P_{\text{rise}} + P_{\text{fall}})}{2}$$

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